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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,263	SENTHILKUMAR ET AL.	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19 and 28-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19 and 28-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9-2-2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19, 28, 32, 35, 40, and 43-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger) in view of Clarke US 6,337,604 (Clarke) and Klughart US 5,546,055 (Klughart '055).

Figures 1 and 2 of Plangger provides for the claimed method steps and apparatus structure that includes includes the step of generating a system time signal using a real time clock circuit composed of at least element 104 that has a tunable oscillator composed of at least element 98 for adjusting an operation frequency of the real time clock circuit. The system time signal is internal to the processor 80 (See column 7). This processor receives a reference time signal over a network. The particular network that Plangger uses happens to be the WWV network. The examiner must give the broadest reasonable interpretation to the claimed invention consistent with the specification. It is accordingly noted that applicant has not defined the term "network" in the specification and thus the common everyday definition of this term applies. Plangger clearly describes in column 8 how the variable capacitance element 98 of the tunable oscillator is controlled so as to adjust the tunable oscillator in order to increase or decrease the operating frequency of the real time clock circuit in response to a difference between the system time signal and the reference time signal. Plangger utilizes a single adjustable capacitor namely a varactor diode 98 to vary the capacitance of the tunable oscillator that generates the real time clock signal used by the processor. Claim 19 now recites a set of control signals to modify the selection of a set of capacitors within a capacitor bank so as to from a variable capacitor used in the real time clock circuit that in turn whose variations correlates to the changes in operation frequency of the real time clock circuit. As evidenced by Clarke, one art recognized variable capacitance structure that is used to control the frequency of an oscillator that is used as a clock is the plurality of independently selectable on-chip capacitors (Note elements C1-C6 and the corresponding control signal D_o-D_5.).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the variable capacitor with one that is composed of a plurality of capacitors each switched by a control circuit like that of Clarke given the art recognized equivalence of these two capacitor arrangements as taught by Clarke.

Plangger and Clarke are also silent on the use of MOSFET capacitors for the capacitors that make up the bank of capacitors.

Figure 9 of Klughart '055 discloses the use of on-chip n-depletion MOSFET load capacitors 1230 and 1232 whose source and drain are clearly connected together as is clearly illustrated. Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '055.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip n-depletion MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors of the combination made obvious above wherein each of these capacitors has a terminal connected to ground given the art recognized equivalents of these capacitor arrangements. as taught by Klughart '055.

The combination above is silent on the exact values of the capacitors that make up the capacitor bank. Specifically having one that is less than 1 pF.

However, the selection of the capacitance values is merely part of the optimum or workable range. The values of the capacitors determines haow many are needed and how great a resolution one can obtain which is all part of the selection of optimum or workable range.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have selected the value of at least one of the capacitances to be less than one pico-Farad (PF) as this is the selection of the optimum or workable range that involves but routine skill in the art.

Claims 29, 30, 31, 36, 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger) in view of Clarke US 6,337,604 (Clarke) and Klughart US 5,546,055 (Klughart '055) as applied to claims 19, 28, 32, 35, 40, and 43-46 above, and further in view of Horn "Basic Electronics Theory" 4th Edition pp 377-378, pp 418-426 and pp 454-465.

All the same reasoning as applied in the 35 USC 103 rejection of claims 19, 28, 32, 35, 40, and 43-46 and the following: Clarke is silent on using buffer circuitry to decouple the switches from the set of memory registers.

Horn teaches that buffers are used to ensure that the output drive is sufficient to drive the devices on the output thereof.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a buffers between the transmission gate switches and the memory registers so as to insure that there is sufficient drive for the transmission gate switches as taught by Horn.

Clarke is likewise silent on the use of filtered power signals to power the buffer circuitry. Buffer circuitry requires a power supply as is well known in the art so that it can provide the sufficient drive as noted above. Horn teaches that it is commonplace to utilize filtered power supplies, in particular note pages 456 and 460 to power electronic devices. This as Horn recognizes reduces "ripple", i.e. noise, or voltage fluctuations that then in turn causes less vacillations in the devices powered by such power supplies.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a filtered power supply to power the buffers made obvious above so as to reduce the introduction of noise in the system as is taught by Horn.

Plangger, Clarke and Klughart are silent on the use of a filter capacitor i.e. low pass filter so to generate a filtered voltage signal to bias the capacitors of the oscillator contains the bias signal and no other unwanted signals like noise, AC components etc..

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted a conventional constant voltage circuit that includes a filter capacitor for the constant voltage circuit of Clarke because, as the reference is silent as to the exact composition of the constant voltage circuit one of ordinary skill in the art would have been motivated to use any art-recognized equivalent constant voltage circuit such as the well-known constant voltage circuit that includes a filter capacitor.

Claims 19, 28, 29, 30-32, 35-40 and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger) in view of Clarke US 6,337,604 (Clarke) and Klughart US 5,8701,411 (Klughart '411) and Horn "Basic Electronics Theory" 4th Edition pp 377-378, pp 418-426 and pp 454-465.

Figures 1 and 2 of Plangger provides for the claimed method steps and apparatus structure that includes includes the step of generating a system time signal using a real time clock circuit composed of at least element 104 that has a tunable oscillator composed of at least element 98 for adjusting an operation frequency of the real time clock circuit. The system time signal is internal to the processor 80 (See column 7). This processor receives a reference time signal over a network. The particular network

that Plangger uses happens to be the WWV network. The examiner must give the broadest reasonable interpretation to the claimed invention consistent with the specification. It is accordingly noted that applicant has not defined the term "network" in the specification and thus the common everyday definition of this term applies. Plangger clearly describes in column 8 how the variable capacitance element 98 of the tunable oscillator is controlled so as to adjust the tunable oscillator in order to increase or decrease the operating frequency of the real time clock circuit in response to a difference between the system time signal and the reference time signal. Plangger utilizes a single adjustable capacitor namely a varactor diode 98 to vary the capacitance of the tunable oscillator that generates the real time clock signal used by the processor. Claim 19 now recites a set of control signals to modify the selection of a set of capacitors within a capacitor bank so as to from a variable capacitor used in the real time clock circuit that in turn whose variations correlates to the changes in operation frequency of the real time clock circuit. As evidenced by Clarke, one art recognized variable capacitance structure that is used to control the frequency of an oscillator that is used as a clock is the plurality of independently selectable on-chip capacitors (Note elements C1-C6 and the corresponding control signal D_0-D_5

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the variable capacitor with one that is composed of a plurality of capacitors each switched by a control circuit like that of Clarke given the art recognized equivalence of these two capacitor arrangements as taught by Clarke.).

Plangger and Clarke are also silent on the use of MOSFET capacitors for the capacitors that make up the bank of capacitors.

Figure 9b of Klughart '411 discloses the use of on-chip p-enhancement MOSFET capacitor 32 whose source and drain are clearly connected together as "common" i.e. conventional (See column 7, around line 18). Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '411.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip p-enhancement MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors Clarke because, as the Clarke reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known on-chip p-enhancement MOSFET capacitors as recited by Klughart '411.

Clarke is silent on using buffer circuitry to decouple the switches from the set of memory registers.

Horn teaches that buffers are used to ensure that the output drive is sufficient to drive the devices on the output thereof.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a buffers between the transmission gate switches and the memory registers so as to insure that there is sufficient drive for the transmission gate switches as taught by Horn.

Clarke is likewise silent on the use of filtered power signals to power the buffer circuitry. Buffer circuitry requires a power supply as is well known in the art so that it can provide the sufficient drive as noted above. Horn teaches that it is commonplace to utilize filtered power supplies, in particular note pages 456 and 460 to power electronic devices. This as Horn recognizes reduces "ripple", i.e. noise, or voltage fluctuations that then in turn causes less vacillations in the devices powered by such power supplies.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a filtered power supply to power the buffers made obvious above so as to reduce the introduction of noise in the system as is taught by Horn.

Plangger, Clarke and Klughart '411 are silent on the use of a filter capacitor i.e. low pass filter so to generate a filtered voltage signal to bias the capacitors of the oscillator contains the bias signal and no other unwanted signals like noise, AC components etc..

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted a conventional constant voltage circuit that includes a filter capacitor for the constant voltage circuit of Clarke because, as the reference is silent as to the exact composition of the constant voltage circuit one of ordinary skill in the art would have been motivated to use any art-recognized equivalent constant voltage circuit such as the well-known constant voltage circuit that includes a filter capacitor.

Claims 33 and 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger) in view of Clarke US 6,337,604 (Clarke) and Klughart US 5,546,055 (Klughart '055) as applied to claims 19, 28 and 32 above, and further in view of Kuhn Jr. US 3,930,169 (Kuhn, Jr.).

Clarke is silent on the composition of the switches 9, 11, 13, 15, 17, 19(a,b) that switches the capacitors in and out of the circuit so as to change the frequency of the oscillator.

Transmission gate switches are conventional switching means as noted by Kuhn, Jr. (See Figure 1 and column 4, lines 3-29).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted conventional transmission gate switches in place of the generic switches of Clarke because, as the reference is silent as the exact switching element employed one of ordinary skill in the art would have been motivated to use any art-recognized equivalent switch such as the well-known, conventional transmission gate switch as taught by Kuhn, Jr..

Note that the circuit of Clarke has a "set of registers" 21 to provide the control signals D0-D5 for selecting the individual capacitors C1-C6.

Claims 34 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable Plangger, Clarke, Klughart and Kuhn, Jr. as applied to claims 33 and 41 above, and further in view of Horn "Basic Electronics Theory" 4th Edition pp 377-378, pp 418-426 and pp 454-465.

Clarke is silent on using buffer circuitry to decouple the transmission gate switches from the set of memory registers.

Horn teaches that buffers are used to ensure that the output drive is sufficient to drive the devices on the output thereof.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a buffers between the transmission gate switches and the memory registers so as to insure that there is sufficient drive for the transmission gate switches as taught by Horn.

As it relates to claim 10, Clarke is likewise silent on the use of filtered power signals to power the buffer circuitry. Buffer circuitry requires a power supply as is well known in the art so that it can provide the sufficient drive as noted above. Horn teaches that it is commonplace to utilize filtered power supplies, in particular note pages 456 and 460 to power electronic devices. This as Horn recognizes reduces "ripple", i.e. noise, or voltage fluctuations that then in turn causes less vacillations in the devices powered by such power supplies.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a filtered power supply to power the buffers made obvious above so as to reduce the introduction of noise in the system as is taught by Horn.

Applicant's arguments with respect to claims 19 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571)272-1770. The examiner can normally be reached on Tues-Fri from 8:30 to 4:30. The examiner can also be reached on alternate Fridays. The examiner normally has second ~~Fridays~~ Mondays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
March 18, 2004
December 24, 2004

Michael B. Shingleton
Primary Examiner
Art Unit 2817